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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/542,674	01/20/2006	John R.A Ayres	GB03 0101 US	1712

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EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	PAPER NUMBER
2816	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

5H

Office Action Summary	Application No.	Applicant(s)	
	10/542,674	AYRES ET AL.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 July 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: C1, C2, R11, and R12 of none of Figs. 4, 7, 9, and 11 are not cited. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: Page 11, line 19 "P_{1a}" should be --N_{1a}--. Page 12, line 19 "36" should be --30--. Clarification is requested with respect to "/Øb" and "Øb" on lines 11 and 15 of page 14. For example, they appear to be reversed with respect to what is shown within Fig. 9. Appropriate corrections are required.

Claim Objections

Claims 7-15 are objected to because of the following informalities: Claim 7, line 5 should have --the-- added prior to "junction node" to clearly relate it back to the "junction node" cited on lines 4-5. For consistent labeling throughout the claims, it is suggested --charge pump-- be added prior to "capacitor" on line 7 of claim 11. Dependent claims carry over any objection(s) upon any claim(s) they depend upon. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2, 4, and 6-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. It is not clear in claim 2 how "an input voltage", "an integer multiple", "a low supply line voltage", and "a high supply line voltage" on lines 4-6 actually relate to "an input voltage", "an integer multiple", "a low supply line voltage", and "a high supply line voltage" cited on lines 2-4, respectively. For example, does each stage have its own distinct input voltage, integer multiple, and line voltages that are different from the other stage? It is not understood in claim 4 if each section increases the same "input voltage", or if they increase their own corresponding input voltage. Similarly, it is not understood in claim 6 if each section decreases the same "input voltage", or if they decrease their own corresponding input voltage. The phrase "the or each charge pump section" within each of claims 7, 8, and 11 is confusing. For example, how does this phrase relate to "at least one charge pump section" cited within claim 3 since "the or each charge pump section of the voltage increasing stage and of the

voltage decreasing stage" on lines 2-3 of claim 7 appears to imply that the voltage decreasing stage has also been identified with at least one charge pump section. However, claim 3 only indicates the section(s) with respect to the voltage increasing stage. Therefore, does the voltage decreasing stage also include the "at least one section" of the voltage increasing stage? It is not clear in claim 8 how the first/second input switches, first/second output switches, first/second junction nodes, and first/second charge pump capacitors all relate to one another, and to the input switch, output switch, junction node, and charge pump capacitor cited within claim 7. For example, the series connected first input/output switches could be connected in parallel with the series connected second input/output switches, or the two sets of series connected input/output switches could actually be connected in series with respect to each other. Claim 11 has the same time of problems as previously described with respect to claim 8. For example, it is not clear in claim 11 how the first/second input switches, first output switch, first/second junction nodes, and first/second (charge pump) capacitors all relate to one another, and to the input switch, output switch, junction node, and charge pump capacitor cited within claim 7. It is not clear in claim 15 how "the charge pump capacitor" and "the capacitor" on lines 2 and 3, respectively relate to the first/second charge pump capacitors cited within claim 8. For example, does this perhaps relate to only a first charge pump capacitor within each of the stages, to a first capacitor in only one stage and a second capacitor in the other stage, or to a second capacitor in each stage? Similar to claim 2 above, it is not clear in claim 16 how "an input voltage", an integer multiple", "a low supply line voltage", and "a high supply line voltage" on lines 4-6 actually relate to "an input voltage", "an integer multiple", "a low supply line voltage", and "a high supply line voltage"

cited on lines 2-4, respectively. Dependent claims carry over any rejection(s) upon which they depend.

Claims 4 and 6 each recites the limitation "the input voltage" in line 3. There is insufficient antecedent basis for this limitation in either claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 5, 7-9, 14-15, and 17-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Myono. Fig. 7 shows a charge pump circuit comprising voltage increasing stage 30 (e.g. see column 10, line 64-65), voltage decreasing stage 50 (e.g. see column 10, lines 65-66), and shared input 1.25Vdd, with respect to block 40. Therefore, claim 1 is anticipated. The combination of diode D2, capacitor C2, and diode D3 within voltage increasing stage 30 is one type of a charge pump section, anticipating claim 3. Similarly, the combination of diode D'3, capacitor C'2, and diode D'2 within voltage decreasing stage 50 is one type of charge pump section, and claim 5 is anticipated. Deeming diode D2 (D'2) as one type of an input switch, and diode D3 (D'3) as one type of an output switch, they are series connected at junction node VH2 (VH'2), wherein charge pump capacitor C2 (C'2) is connected between junction node VH2 (VH'2) and a control line (i.e. the output of driver 31b (51b)), claim 7 is anticipated. In another

interpretation of what is shown/ understood from Fig. 7, the charge pump section of voltage increasing stage 30 (50) comprises first input switch D1 (D'1) in series with first output switch D2 (D'2) connected together at first junction node VH1 (VH'1); and second input switch D3 (D'3) in series with second output switch Dn+1 (D'n+1) connected at second junction node (unlabeled, but understood). With first charge pump capacitor C1 (C'1) connected between first junction node VH1 (VH'1) and a first control line (i.e. the output of driver 31a (51a)), and second charge pump capacitor C3 (C'n) connected between the unlabeled junction connection and a second control line (i.e. the output of driver 31b (51c)), claim 8 is anticipated. Although not clearly identified as complementary signals, Myono discloses the use of clocks with reverse phase clock pulses (e.g. see columns 1 (line 62), columns 4 (lines 4-6), 5 (lines 18-20), and 7 (lines 48-49)). Therefore, it would be understood by one of ordinary skill in the art that these signals are complementary, anticipating claim 9. The complementary signals would effectively allow the first input/output switches to operate in a complementary manner, anticipating claim 14. When a clock driver (e.g. one of 31a-31b) of voltage increasing stage 30, and a clock driver (e.g. one of 51a-51c) of voltage increasing stage 50 each provide a low (or high) output at the same time, their corresponding charge pump capacitors are effectively connected together (i.e. connected to the low (or high)). This anticipates claim 15. Whether deeming 30-50 as an electronic device, or 30-50 being used in a larger system that is one type of an electronic device, claim 17 is anticipated. Myono discloses the use of switching regulators/voltage generators (e.g. the charge pump circuit) with respect to liquid crystal displays (e.g. see column 1, lines 29-31). Therefore, it would be understood by one of ordinary skill in the art that the larger electronic

device, including the circuit of claim 1, could comprise a liquid crystal display, anticipating claim 18.

Claims 1, 3, 5, and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Morishita. Fig. 2 shows a charge pump circuit comprising voltage increasing stage 4 (e.g. see column 8, lines 15-19), voltage decreasing stage 2 (e.g. see column 8, lines 6-10), and shared input VREF, thus anticipating claim 1. 4 and 2 can each be considered at least one charge pump section for stages 4 and 2, respectively, anticipating claims 3 and 5. The overall circuit shown in Fig. 2 is one type of electronic device, and claim 17 is anticipated.

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 4, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morishita as applied to claims 1, 3, and 5, respectively described above. Although Morishita

shows/discloses a charge pump circuit comprising the stages and shared input as recited within claims 1, 3, and 5, the reference does not clearly show or disclose increasing/decreasing an input voltage by an integer multiple of the difference between low and high power supply line voltages, or each stage comprising a plurality of sections, wherein each section increases the input voltage by the difference described above. It would have been obvious to one of ordinary skill in the art to either add additional stages to the overall circuit, or each of stages 2 and 4 with either a doubler, or another type of multiplying, stage. For example, one stage could be used to double, or provide another desired integer multiple of, a difference between a low supply line voltage (e.g. ground) and a high supply line voltage (e.g. VEX), wherein another stage could be used to provide a corresponding voltage having the same magnitude, but with an opposite polarity. This renders claim 2 obvious. One of ordinary skill in the art would understand the additional stages, or the replacement stages, can be used to provide the desired output voltages to meet the requirements of the circuitry receiving the output voltages. For example, if the circuitry did not require VBB to be –1.0V, and VPP to be 3.6V (e.g. as disclosed on column 8, lines 9 and 17-18, respectively), suitable stages could be used to provide desired levels of -6.6V and 6.6V if those levels would be required. Also, it would be obvious to one of ordinary skill in the art that if even higher multiples of an input voltage is desired, a plurality of charge pump sections could be coupled in series to provide the increased (or corresponding decreased) output voltage. For example, a first voltage doubler could be used to provide an output voltage of 6.6V with respect to VEX = 3.3V, while a second voltage doubler, coupled in series with the first voltage doubler, could provide a corresponding final output voltage of 13.2V. Therefore, claims 4 and 6 are rendered obvious. The number of charge pump sections (e.g. 1, 2, or more), and their

type (e.g. doubler or tripler), would depend on what final output voltages are desired, and what the initial voltage is that needs to be converted to a higher multiple, and its negative equivalent.

Claims 10 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Myono et al. (Myono) as applied to respective claims 8 and 18 above. Although Myono shows/ discloses the use of complementary/reverse signals as described above with respect to claim 9, and it's understood an electronic device can include the charge pump circuit as recited within claim 18, the reference does not clearly show or disclose the use of non-overlapping signals, or that the circuit and a TFT switching array are provided on a common substrate. It would have been obvious that the complementary/reverse signals of Myono could be non-overlapping signals applied to the first/second control lines, rendering claim 10 obvious. The use of non-overlapping signals would provide one way to minimize having both the input/output switches conducting at the same time. One of ordinary skill in the art would understand that Myono's circuit can utilize MOS transistors (e.g. the diodes, switches and clock driver can be formed from MOS transistors (see column 4, lines 55-62 and column 10, lines 35-43)). Liquid crystal displays typically comprise a switching array, such as thin film transistors (TFT)) to control the pixels and display. Therefore, it would have been obvious to one of ordinary skill in the art to provide the circuit and a TFT switching array on a common substrate, rendering obvious claim 19. This arrangement would provide similar operating characteristics (e.g. temperature, voltage, and current) between the transistors within the switching array and the circuit; minimize the area and power consumed by the transistors/circuit; and be fabricated more easily since the transistors could be formed/ manufactured during the same processes.

No claim is allowable as presently written.

Allowable Subject Matter

However, claims 11-13 would be allowable if rewritten to satisfactorily overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. There is presently no motivation to modify or combine any prior art reference(s) to ensure the charge pump stage comprises the switches, nodes, capacitors, and control lines as recited within claim 11, wherein the second junction node is connected to the second input switch and the second capacitor, and also provides the control signals for the first input/output switches. Claims 12-13 depend on claim 11, and thus carry over its rejections.

Prior Art

The other prior art reference cited on the accompanying PTO-892 is deemed relevant to at least sections of the claimed invention. Although not used in any formal rejection described above, the reference of Komori could have been used to reject at least claim 1. For example, Fig. 1 shows a charge pump circuit comprising voltage increasing stage 31 and voltage decreasing stage 32 sharing input VL1,a (e.g. see column 4, lines 49-52). Komori also discloses that the stages are voltage doublers (i.e. one type of an integer multiplier) on at least lines 49-51 of column 4; and column 5, lines 9-15 disclose that additional stages with different levels can be added, and/or instead of using the voltage doublers, other types of multiplier circuits can be used. Therefore, this reference should be carefully reviewed and considered.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal, can be reached on (571) 272-1769.

The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

22 March 2007

/Kenneth Wells/

Kenneth B. Wells
Primary Examiner